Serial No.: 09/644,464

REMARKS

Claims 1, 3-14 and 16-23 are pending in the application. Claims 1, 3, 4, 7, 10, 14, 16, 17 and 20 have been amended herein. Claims 2 and 15 have been canceled. Favorable reconsideration of the application, as amended, is respectfully requested.

I. REJECTION OF CLAIMS 1-23 UNDER 35 USC §112, 2nd ¶

Claims 1-23 stand rejected under 35 USC §112, second paragraph, as being indefinite. Specifically, the Examiner notes that the claims are indefinite with respect to points a (i thru iv) and b (i thru viii) as set forth on pages 2-3 of the Office Action.

Regarding points a (i thru iv) and b (i, ii and viii), the claims have been amended as noted above in order to address the Examiner's concerns.

As for points b (iii thru vii), the Examiner indicates that claim 10 does not clearly indicate which particular component is carrying out the stated steps. However, applicants respectfully submit that claim 10 is a method claim. As such, applicants further submit that it is not necessary to define in the method claim the particular structures or components which carry out the recited steps. A method claim merely requires a recitation of process steps necessary for the invention.

For at least the above reasons, applicants respectfully request that the rejection of claims 1-23 be withdrawn.

II. REJECTION OF CLAIMS 1-23 UNDER 35 USC §102(b)

Claims 1-23 further stand rejected under 35 USC §102(b) based on *Firoozmand et al.* Withdrawal of this rejection is respectfully requested for at least the following reasons.

Claims 1 and 14 have been amended to incorporate the features of dependent claims 2 and 15, respectively. Claims 1 and 14, as amended, recited the feature of the invention whereby the priority resolution circuit continually retrieves data from the register to determine a highest priority data frame in the buffer memory and *replaces*

the address previously provided to the frame transmission circuit if a higher priority frame becomes available. Similarly, claim 10 recites a method which includes *overwriting the address of the highest priority data frame with an address of a new highest priority data frame if a new higher yet priority data frame becomes available.*

As is discussed in the background section of the present application, it is known to prioritize data frames within a queue.

> However, simply prioritizing frames within a queue does not resolve a front of line blocking problem. A front of line blocking problem occurs when, for example, the highest priority data frame (say priority 3) is retrieved from a queue and is written to a register (or other memory) for transmission in the next available time slot (e.g. interval of time available to the media access controller for transmission). At this time, that data frame is isolated from the remaining data frames left in the queue. The remaining data frames in the queue may be reprioritized with newer, incoming data frames, however, no other frames can be transmitted until that first data frame is transmitted. Hence, a higher priority data frame (say 6) which has come into the queue after the first frame was written to the register is blocked from transmitting before the lower priority data frame 3. (Specification, page 2, lines 17-27).

The present invention as recited in claims 1, 10 and 14 overcomes such problem associated with front of line blocking by virtue of a priority resolution circuit continually retrieving data from the register to determine a highest priority data frame in the buffer memory and replacing the address previously provided to the frame transmission circuit if a higher priority frame becomes available.

Firoozmand et al. does not teach or suggest a system or method which involves a priority resolution circuit continually retrieving data from a register to determine a highest priority data frame in the buffer memory and replacing the address previously provided to the frame transmission circuit if a higher priority frame becomes available as recited in claims 1, 10 and 14. *Firoozmand et al.* does not address the front of line blocking problem with which the present invention is concerned.

Rather, *Firoozmand et al.* is concerned with a different kind of problem relating to "lock up". Specifically, the FIFO memory "locks up" when the amount of storage remaining available in the logical FIFO containing the queue, is less than the storage

capacity of the physical FIFO. (Col. 2, lns. 17-23). *Firoozmand et al.* describes a network DMA controller 124 designed to monitor the FIFO queue. If a queue becomes full, the packet buffer management circuit 156 locks the queue to finish emptying the current FIFO and to suspend the queue. If a transfer is incomplete, the circuit 156 continues with other pending transfers until receiving a signal that the queue becomes unlocked.

In rejecting claims 2 and 15 which originally recited the aforementioned features of the invention, the Examiner pointed to Column 13, lines 13-17 of *Firoozmand et al.* as teaching such features. However, such disclosure in *Firoozmand et al.* simply relates to the priority at which packets are transmitted. Specifically, *Firoozmand et al.* describes how, when the transmitting device receives the token, the transmitting device transmits the synchronous data first. This is because the synchronous data has higher priority than non-synchronous data. Such transmission of the synchronous data before non-synchronous data based on priority is very conventional and not the focus of the invention. The invention relates to the front of line blocking problem that can result from such priority based data transmission.

In particular, *Firoozmand et al. may arguably* teach or suggest a transmission device in which (i) a priority resolution circuit reads a register to determine a highest priority data frame available for transmission; and (ii) a frame transmission circuit receives an address of the highest priority data frame from the priority resolution circuit, receives a signal from a media access controller indicating that a data frame may be transmitted, retrieves a data frame from the buffer memory corresponding to the address, and makes the data frame available to the media access controller for transmitting to the network medium. However, *Firoozmand et al.* does not teach or suggest such a priority resolution circuit *continually retrieving data from the register* to determine a highest priority data frame in the buffer memory *and replacing the address previously provided* to the frame transmission circuit *if a higher priority frame becomes available*.

Consequently, *Firoozmand et al.* does not teach or suggest the invention as set forth in claims 1, 10, 14 and the claims dependent therefrom. Withdrawal of the rejection is respectfully requested.

III. CONCLUSION

Accordingly, all claims 1-23 are believed to be allowable and the application is believed to be in condition for allowance. A prompt action to such end is earnestly solicited.

Should the Examiner feel that a telephone interview would be helpful to facilitate favorable prosecution of the above-identified application, the Examiner is invited to contact the undersigned at the telephone number provided below.

Should a petition for an extension of time be necessary for the timely reply to the outstanding Office Action (or if such a petition has been made and an additional extension is necessary), petition is hereby made and the Commissioner is authorized to charge any fees (including additional claim fees) to Deposit Account No. 18-0988.

Respectfully submitted,

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